AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning on page 4, line 3 with the following paragraph:

[0009] Laterally between the source and drain terminals 38, 40 of both of the D-mode and E-mode transistors 2, 3 is a metal gate contact of the respective transistor 2, 3. The D-mode and E-mode gate contacts 30, 34 are disposed in respective D-mode and E-mode gate recesses 32, 36 that extend into multi-layer substrate 5 from the upper surface of ohmic contact layer ~~90~~ 28. The D-mode and E-mode gate contacts 30, 34 are coupled to different ones of the interior semiconductor layers of multi-layer structure 5 at points vertically below the ohmic contact layer ~~90~~ 28.

Please replace the paragraph beginning on page 5, line 3 with the following paragraph:

[0012] As shown in FIG. 1, the E-mode gate recess 36 and the E-mode gate contact 34 extend vertically deeper into multi-layer structure 5 than the D-mode gate recess 32 and D-mode gate contact 30, because the E-mode barrier layer ~~28~~ 18 to which the E-mode gate contact 34 is coupled vertically below the D-mode barrier layer 22 and the E-mode etch stop layer 20.

Please replace the paragraph beginning on page 7, line 21 with the following paragraph:

[0019] The performance of the E-mode transistor 3 also is compromised in the conventional design. For instance, a certain degree of overetch is required to ensure that the E-mode etch stop layer 20 is reached during the step of etching through D-mode barrier layer 22. During the overetching step, etching in the vertical direction proceeds slowly because of the selectivity of the etchant to E-mode etch stop layer 20. On the other hand, etching in the lateral direction through the D-mode barrier layer 22 proceeds unabated. As a result, the perimeter of the partially-completed E-mode gate recess 36 at the exposed surface of the E-mode etch stop

layer 20 is greater than desired. The subsequent etch step that etches through E-mode etch stop layer ~~50~~ 20 therefore exposes a larger-than-desired area of the upper surface of E-mode barrier layer 18. Since the E-mode gate contact 34 only partially covers the exposed upper surface of the E-mode barrier layer 18 within E-mode gate recess 36, an ungated region 44 on the surface of E-mode barrier layer 18 is formed. Control of the extent of the ungated region 44 is difficult due to variations in the epitaxial layer thicknesses and etch dependencies on the feature size.

Please replace the paragraph beginning on page 18, line 25 with the following paragraph:

[0050] In an exemplary process, the ohmic contact layer ~~90~~ 28 of multi-layer substrate 105 preliminarily is overlaid with a blanket first dielectric layer 301, as shown in FIG. 3A. The dielectric layer 301 may be a layer of silicon dioxide (SiO_2) or silicon nitride (Si_2N_3) deposited using a plasma-enhanced chemical vapor deposition (PECVD) process.